AMENDMENTS TO SPECIFICATION

Page 1, lines 15-23:

In DRAM process, such a condition also happens. With reference to Fig. 2, which is a schematic top view of a gate region structure of a DRAM, reference number 20 indicates an active area, 21 indicates a gate line, 24 indicates a deep trench. As shown in the drawing, the adjacent portion between the active areas is short. Reference number 23 indicates a void formed in the dielectric filled in the STI between the active areas 20. The existence of the void 23 may influence the electric performance of the semiconductor structure. However, such a void is very small and is hardly found during the process. Usually, the existence of the void only can be found in the electric testing, for example, testing of voltage (potential, current, resistance, inductance, or capacitance between two gate lines 21, which is performed after the wafer is finished, cut into chips and packed. Accordingly, a waste of process is generated.

Page 2, lines 3-10:

According to an aspect of the present invention, a shallow trench isolation void detecting method for a semiconductor wafer comprises steps of assigning a testing region in a predetermined region of the semiconductor wafer; forming active areas and gate lines ~~inter~~ associated with the active areas in said detecting region by a synchronous process for other regions, filling a trench between the active areas with dielectric, the adjacent portion between the active areas having at least a predetermined length; and detecting the electric values of the gate lines to determine whether there is a void formed in the dielectric filled in the trench between the active areas.

Page 3, lines 2-12:

As shown in Fig. 3, the sections of active areas 30 in the testing region are formed as long strips. Accordingly, the active areas 30 are adjacent to each other. Shallow trenches formed between the active areas 30 are filled with dielectric 32 by the process synchronous with other portions of the wafer. As shown, in the present embodiment, the active areas 30 are preferably

formed as parallel strips. Since the length of the portions of two active areas 30 adjacent to each other is very long, if the re is void 33 formed in the dielectric 32, the void 33 will be a long void. Gate lines 31' in the testing region are arranged at an interval the same as the gate lines in other non-testing regions. As shown, since the section of the void 33 is long, the void 33 crosses at least two gate lines 31'. Accordingly, for example, it is easy to detect whether there is avoid existing by performing a electric test such as measuring potentials of the gate lines 31' in the testing region, for example, by measuring the potential between two gate lines 31' with a proper voltage applied thereto to obtain a value other than 0 if the void 33 exists, and a value 0 if the void 33 does not exist.

Page 3, lines 13-16:

According to the present embodiment, for the sake of convenience of measuring, the gate 31 can be formed as a comb-shaped gate. That is, the odd gate lines are connected together, while the even gate lines are connected together, thereby forming a dual-comb structure. Then the potential of a plurality of gate lines can be measured at ~~a~~the same time, for example by using the above described electric test.